Dependence of the Fracture of PowerTrench MOSFET Device on Its Topography in Cu Bonding Process

Manmohan Daggubati, Q. Wang, Y. V. Sokolov, Yong Liu, *Senior Member, IEEE*, and Lu-Chang Qin

***Abstract*—Dependence of the fracture-resistance of a PowerTrench MOSFET device on its topography in Cu bonding process was investigated. Two different topographies, namely dimple and round, have been tested. A significantly higher cratering rate has been clearly observed on dimple topography. The dimple topography exhibited a cratering rate of 371 k ppm levels compared to 0 ppm in round topographies. Three-dimensional nonlinear finite-element analysis has shown that the largest compressive and shear stresses and their locations were identified, respectively, in borophosphosilicate glass (BPSG)/barrier metal layers of the dimple topography. The round topography had the smallest stress in BPSG/barrier metal layers. The higher compressive stress transferred to silicon in the dimple topography during the bonding process can induce a local crack, consequently causing silicon fracturing during the shearing processes. A significant improvement in the cratering performance was observed when the Al bond pad metal layer was reinforced by adding a barrier layer sandwiched in the Al metal layers. The cratering rate decreased to 1300 ppm levels. Additionally, the change in composition of a BPSG layer caused cratering was briefly discussed and an oxygen rich BPSG film in round topography was confirmed by the energy dispersive spectroscopy (EDS) of a cross-sectional TEM sample. It has been found that the cratering rate on dimple topography significantly increased from 1 k ppm to 100 k ppm levels, when the resulting residual Al pad thickness is less than 0.65 μm for Cu bonding performed with different ultrasonic (US) power and bond forces.**

***Index Terms*—Bonding, cratering, borophosphosilicate glass (BPSG), device fracture, metal–oxide–semiconductor field-effect transistor (MOSFET), topography.**

I. Introduction

THE Cu bonding process has increasingly been adopted in the semiconductor industry for its economy and superior electrical conductivity [1]–[5] with respect to Au as well as for its mechanical resistance to wire sweep during plastic encapsulation [6], [7]. Additionally, the Cu wire/Al bond is more reliable and less sensitive to temperature degradation. As a result, Cu wire bonding has been widely employed in high current packages for power devices. However, when bonding Cu to Al metal pad in devices, harder Cu has a tendency to displace the softer Al pad metal and causes silicon fracturing. One of the signatures of this mechanical damage, termed cratering, is visible cracking and chipping of silicon. Extensive characterization has been done on Cu bonding-related die cracking or cratering. Harman *et al.* [8]–[10] has indicated that bonding process parameters, such as ultrasonic (US) power, free air ball (FAB) size, and forming gas are crucial on die cratering; while Mori [9] and Tomlinson [11] have shown that die cratering can be reduced by using a pad metal with an appropriate hardness. Some additional studies have also been done in quantifying the effects of Al–Cu intermetallics and other thermal stresses in the thin metal/borophosphosilicate glass (BPSG) layers [12]–[14]. Though, optimization of Cu wire bonding parameters has significantly improved the cratering performance in the past twenty years; most of these studies were performed on integrated circuit (IC) devices where at least three or more metal/dielectric interconnect layers exist between the pad metal and the silicon device. In power discrete devices, on the contrary, the pad metal is separated from the silicon device only by one BPSG layer. The reduced structure of the discrete device may exhibit different Cu bonding performances from IC devices. The discrete device may be more susceptible to the Cu bumping process. For example, the device cratering may be very sensitive not only to the Cu bonding process, but also to the underlying device topography and the mechanical properties of the BPSG layer.

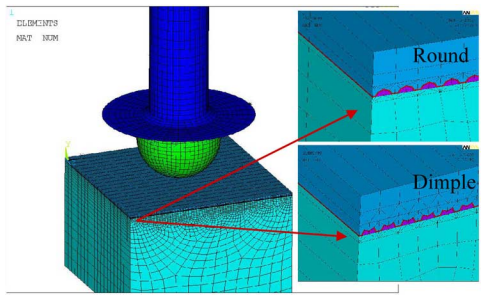

Fig. 1. 3-D FEM mesh showing Cu bonding process for round and dimple topographies.

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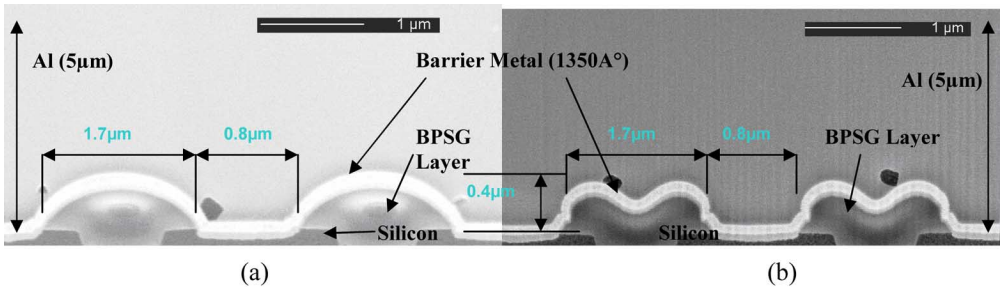

Fig. 2. Cross-sectional SEM images of (a) round and (b) dimple topographies showing aluminum, barrier metal and BPSG layers with their dimensions.

This paper addresses some aspects of the relationship between the device topography and its fracture strength in the copper wire bonding process. The cratering performance of different device topographies has been characterized with a standard Cu bonding processes. The stress in silicon devices with those topographies have been analyzed with finite-element analysis (FEA) and compared to the experimental cratering data of the devices. This investigation has also explored the dependence of residual Al thickness on Cu FAB size and the effects of the reinforced Al pad metal and its impact on silicon cratering.

II. Experimental Work

The device topographies were controlled by interlayer BPSG dielectric film deposited by PECVD. Different topographies were manufactured by varying both SiH_4 to N_2O flow rate ratio during the BPSG film deposition and the film thickness. The changes in the film thickness and flow property made the desired topographies realizable. The BPSG film was then selectively etched and deposited with sputtered barrier metal ($\sim$1350 Å) and Al ($\sim$5 μm) bond pad metal layers. Cu wire bonding procedure is as follows. The copper wire is fed through a capillary and an electronic flame-off (EFO) spark melts the wire forming a Cu ball (free air ball or FAB). The Cu wire with the FAB is then lowered to the heated bond pad and is pressed against it. To ensure a good bonding, an ultrasonic power is also applied to the Cu-wire during this stage. Then the capillary is raised, and moved to the left for the wire clamp to shear the wire and finally the wire breaks during the pull. Copper wires of 76.2 μm in diameter were used. The N_2+H_2 gas mixture was used to prevent oxidation during copper ball formation and bonding. Ball bonding was also done with different FAB sizes (190 and 145 μm), US power and bond force settings to study their effects on the cratering. The residual Al thickness underneath Cu bump was measured from cross-sectional scanning electron microscope (SEM) images after the bonding process. Aqua regia etch was used to analyze under bond pads for fringing or cratering. 3-D FEA was used to simulate the compressive/tensile/shear stresses induced in these test device structures during the bonding process (Fig. 1). To further improve the bond pad metal strength, a sandwich metal pad structure of Al/TiW/Al was created. The film thicknesses were 2.5 μm, 1350 Å, and 2.5 μm, respectively.

III. Results and Discussion

Two device topographies have been created in our experiment (Fig. 2). The round topography device topography in Fig. 2(a) was made possible with higher SiH_4/N_2O ratio; the low SiH_4/N_2O ratio led to a dimple topography device topography in Fig. 2(b). The height and width of both topographies were the same and were approximately 0.4 μm and 1.7 μm, respectively. The distinctive effect of two topographies on cratering behavior has been observed. Within 4864 dies tested, the dimple topography exhibited a cratering rate $>$ 371 k ppm, compared to a 0 ppm on the round topography (Table I). An SEM top view image of the cratered dies from the dimple topography shows a typical silicon cratering signature (Fig. 3) that is consistent with previous studies [10], [11]. Further experiments show that the dimple topography with the same width but a reduced height (Fig. 4) has significantly reduced cratering rate. Tested on 4864 sample dies, reducing the height of the dimple topography to 0.2 μm decreased the die cratering rate from 371 k ppm to 17 k ppm (Table I). This indicates that both the topography and large aspect ratio (height/width $>$0.12) induce stress concentrations large enough for cratering.

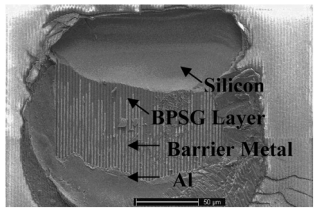

Fig. 3. SEM top-view of a typical silicon crater showing different exposed layers under the aluminum bond pad metal.

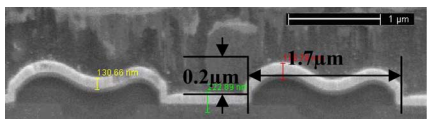

Fig. 4. SEM cross-section of a reduced dimple topography (reduced in height).

It is well understood that the silicon cratering shown in Fig. 3 tends to occur when large mechanical stresses are transferred directly into the silicon during the Al pad deformation by bonding the Cu ball [11]. Large Al deformation can result in the Cu ball in the vicinity or in contact with the barrier metal/BPSG film layers. In the dimple structure, due to the sharper corners on its top surface region, a local mechanical stress concentration has been realized as shown in the stress contours given by FEA study (Fig. 5). This stress concentration leads to a higher mechanical stress in the silicon at the barrier/BPSG contact edges.

TABLE I
DESCRIPTION OF SAMPLES, ASPECT RATIO, SAMPLE SIZE, AND THE CRATERING RATES OF DIFFERENT TOPOGRAPHIES

Sample Description	Aspect ratio	# Die samples	Bond crater (PPM)
Dimple	0.24	4864	371429
Reduced Dimple	0.12	4864	17681
Round	0.24	4864	0
Dimple with 2000A° barrier metal layer	0.24	4864	564286
Dimple with 1350A° reinforced layer	0.24	4864	1300

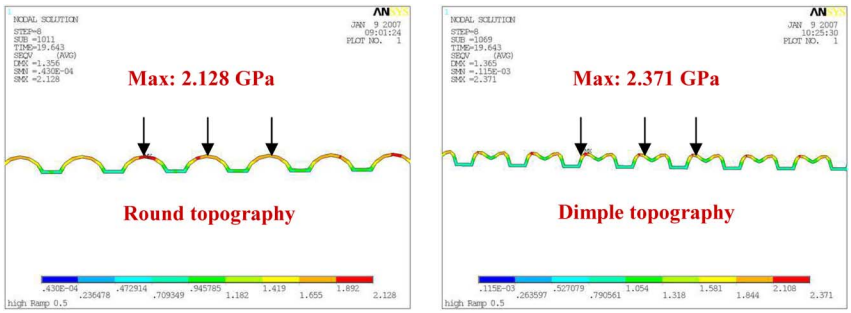

Fig. 5. Stress in barrier/dielectric layers, showing maximum stress concentrations at the top surface region of the barrier metal layer.

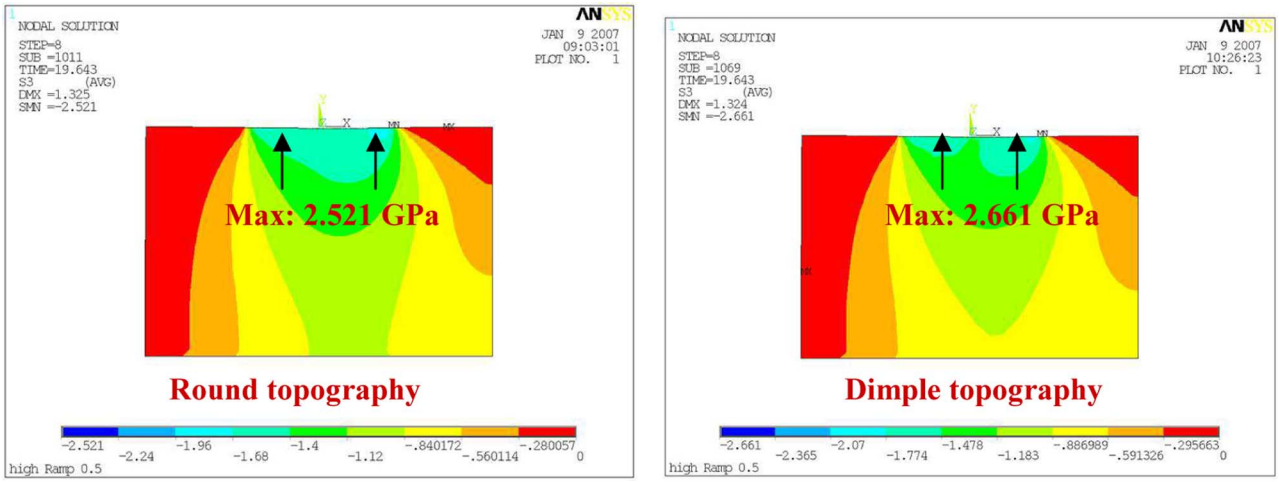

Fig. 6. Stress contours in silicon during Cu bonding process for both round and dimple topographies.

Since stress level is a determining factor to the cratering mechanism of the device, these high-stress locations are considered to be preferential for the crack initiation and cratering in the bonding process. The simulation further shows that a compressive stress of 5.64 GPa and a shear stress of 1.21 GPa are induced in the BPSG/barrier metal layers of the dimple topography. The corresponding stresses are 3.84 GPa and 1.0 GPa, respectively, for the round topography. Also, the compressive stress transferred to the silicon is found to be 2.66 GPa for the dimple and 2.52 GPa for the round topographies (Fig. 6). Though simulated stress values may not reflect the actual stress values due to the assumptions and limits in model inputs, it is clearly seen that the dimple topography leads to much larger compressive stresses in both BPSG layers and silicon than those in the round topography. This trend is consistent with the experimental results. For the dimple topography, even the dies that marginally passed the bonding tests exhibited micro-cracks and craters (Fig. 7). These micro-cracks can also be considered as crack nuclei, which lead to cratering on majority of the other dies with the same topography. The locations of these micro-cracks are also consistent to the locations of higher stress in FEA stress contours analysis (Fig. 6).

Furthermore, from the energy absorption standpoint, the dimple topography confines the Al pad metal from displacing during Cu bonding, thus transferring all the Cu ball impact energy downwards into the silicon. In the case of the round

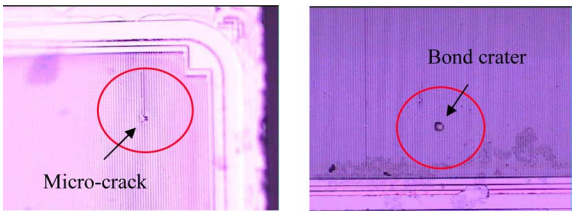

Fig. 7. Micro-cracks and bond craters on silicon observed after etching the top metal and dielectric layers with aqua regia.

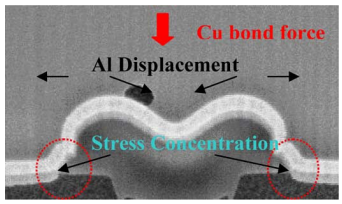

Fig. 8. SEM image illustrating the possible mechanism of aluminum displacement and stress concentration points for a dimple topography.

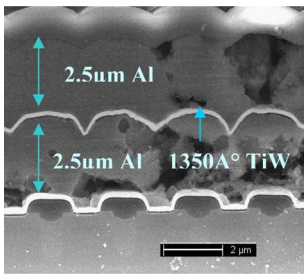

Fig. 9. SEM cross-sectional image of the aluminum/TiW/aluminum sandwich for strengthening the bond pad metal.

topography, the reduced surface topography offers minimum resistance to displacing Al or yielding to the bond stress, which may facilitate more impact energy absorption by the Al pad layer as shown in Fig. 8. This consideration is also supported by the reduced cratering rate observed on the dimple topography with the reduced aspect ratio (Fig. 4). The reduced aspect ratio of the dimple topography has less resistance for Al displacement.

To reduce the impact force or compressive stress on the dimple topography devices during Cu bonding, further experiments were conducted with the increased thickness of the protective barrier metal layer. When it is increased from 1350 Å to 2000 Å, no improvement in cratering performance was observed. A very high cratering rate of ∼564 k ppm was still observed on these dies as shown in Table I. However, when the barrier metal layer is sandwiched between two 2.5 μm Al-pad layers, bonding performed on the dimple structures showed a significant improvement in the cratering performance (Fig. 9). With a 1350-Å thick barrier metal (reinforced layer), the cratering rate decreased to 1300 ppm levels on a sample size of 4864 dies. When the thickness of the reinforced layer increased to 2000 Å, no further improvement in the cratering rate was observed. These results can be explained that thicker barrier metal layer will only reduce the compressive deformation but not the shear or tensile stresses which are also important in both crack nucleation and growth.

The silicon cratering in the dimple topographies can also be affected by the BPSG composition itself. The dimple and the round topographies are the results of the BPSG films being more and less viscous, respectively. When the ratio of SiH_4 to N_2O flow rates was varied to produce the topographies, the film composition could change significantly resulting in different flow ability and different mechanical properties such as elastic modulus of the BPSG [15]. The BPSG compositional change has been verified by the means of selective energy-dispersive spectroscopy (EDS) on the transmission electron microscope (TEM) cross-sectional samples of both topographies as shown in Fig. 10. The round topography exhibited higher oxygen to silicon ratio $(O/Si \sim 5.3)$ compared to the dimple topography $(O/Si \sim 3.2)$, indicating the stoichiometry of the oxides are different. The BPSG film in the dimple structure being less elastic will undergo higher compressive stress in the center and tensile at the edges leading to cracking [16], whereas the less viscous film in the round structure will reduce the magnitude of the stress by plastic deformation [14]. Therefore, it is likely that different elasticity and Young's moduli in BPSG layers can transfer different mechanical stresses in the underlying silicon leading to cracking and eventually complete failure of the device. Additional experiments are needed to study this effect.

Additional experiments on the dimple device topography showed the relationship between cratering rate and the residual Al thickness regardless of bonding parameters (ultrasonic power, bond force, and FAB size). The cratering rate decreases exponentially from 100 k ppm to 1 k ppm levels when the residual Al thickness is more than 0.65 μm after the Cu bonding process [Fig. 11(a)], i.e., a minimum residual Al thickness exists for low cratering rate in the device with dimple topography. No such relationship has been observed for the round device topography [Fig. 11(b)]. Previous study has shown that the residual Al thickness is a function of bonding force, ultrasonic power, and ultrasonic amplitude [11]. The bonding force determines exclusively the compressive stress in the silicon. When the bonding force exceeds a certain value, it will create crack nuclei in the silicon as shown in Fig. 7. The subsequently applied ultrasonic vibration will grow the crack. When the crack size is less than the critical value for the given shearing process, the Cu wire shearing will not lead to any silicon cratering as shown in Fig. 3; while the crack size is larger than the critical size, the shearing process will result in the silicon cratering. The observed minimum Al residual thickness for the dimple topography is therefore related to the initial critical size of the crack produced by the Cu wire bonding force and ultrasonic vibration. The residual Al thickness has also been found directly proportional to the FAB size [Fig. 10(a)]. The residual Al pad thickness decreased from 2 to < 0.5 μms with decrease in FAB size from 170 (FAB3) to 130 μms (FAB1) as shown in Fig. 10(a). This is consistent to our simulation results that show significantly lower stresses generated by FAB size of 190 μm compared to the FAB size of 145 μm for the same topographies. It is clear that for the dimple topography, optimized Cu bonding process should result in a minimum residual Al thickness that is 0.65μm in our experimental conditions [Fig. 11(a)]. When Cu ball is bonded to Al pad with excessive force, the impact causes the Al metal to extrude to the bond

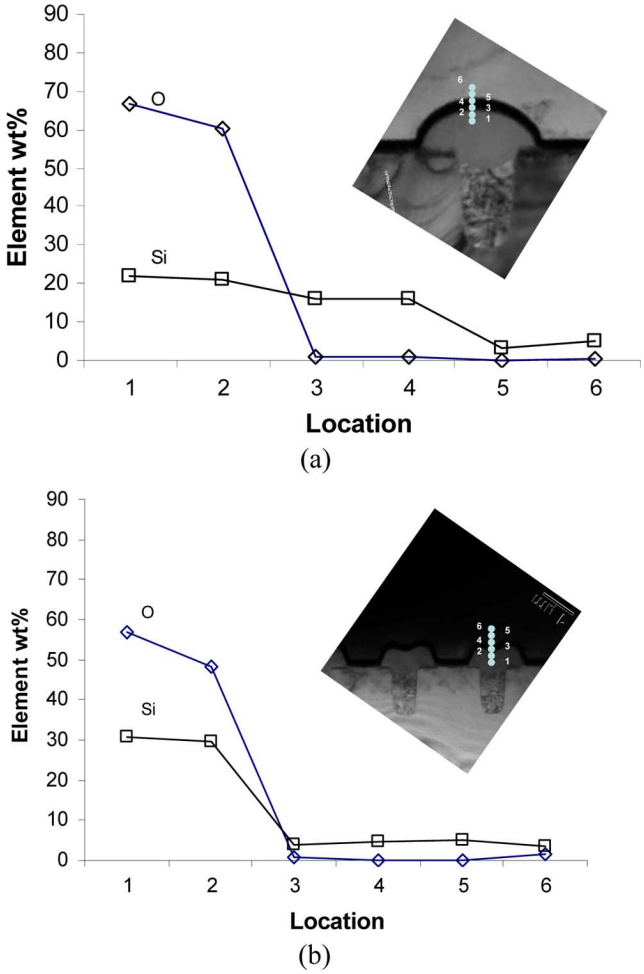

Fig. 10. EDS spectra of oxygen and silicon elemental weight percent at different locations on a cross-sectional TEM sample of (a) round and (b) dimple topography.

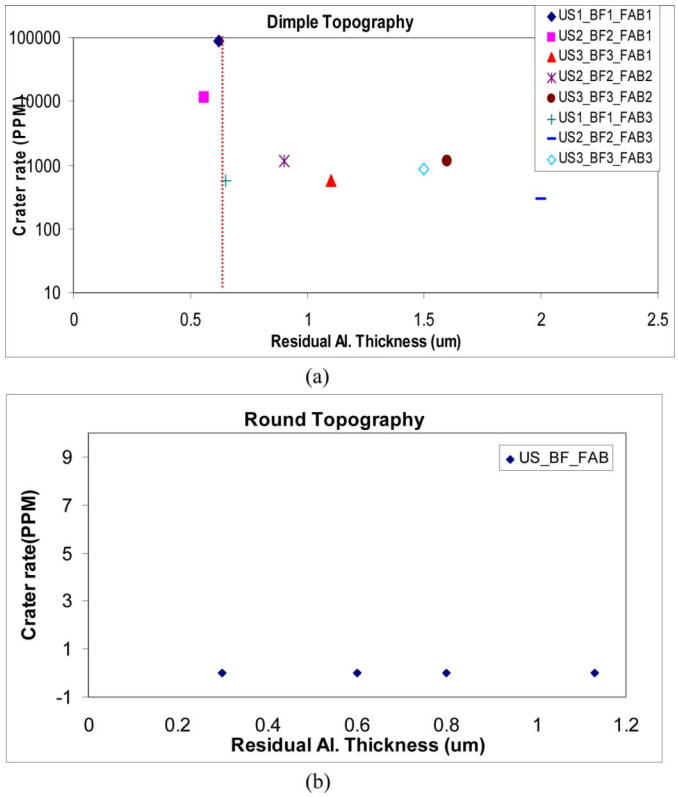

Fig. 11. Cratering rate versus residual aluminum cap thickness for (a) dimple topography with different bond settings and (b) round topography with optimized bond setting.

corners/periphery. It is commonly referred to as overbonding in the industry [11]. This can weaken the ball-to-pad adhesion and lead to dielectric cracking or silicon cratering. The thickness of the Al bond pad mainly serves to absorb the impact energy during the Cu wire bonding process. The dimple topography confines the Al pad metal from displacing during Cu bonding and thus transfers all the Cu ball impact energy into the silicon, resulting in the relationship between cratering rate and the residual Al thickness. In contrary, the smooth topography of round topography enables an easier Al displacement, which absorbs most of the impact energy. The round topography leads to less stress transferred into the silicon and significantly reduced cratering rate even with the residual Al thickness much less than 0.65 μm [Fig. 11(b)]. The remaining cratering rate of $\sim$1 k ppm observed across all the samples with residual Al thickness > 0.65 μm could still be due to the stress concentration factor of the dimple topography discussed earlier. Thus, the generation of higher silicon stresses via topography and/or bonding parameters plays a significant role in cratering.

IV. Summary

Cratering rate was found to be significantly dependent on the device topography. The dies with dimple topography exhibited a cratering rate of 371 k ppm, whereas the round topography yielded zero craters. Higher mechanical stress concentrations in the dimple topography were found to be responsible for causing cratering in the underlying silicon. FEA showed a higher compressive and shear stress of 5.64 GPa and 1.21 GPa, respectively, on a dimple topography, as compared to 3.84 GPa and 1.0 GPa on a round topography. The simulated compressive and shear stresses in silicon on dimple topographies exceed the compressive strength (1 GPa) and tensile stress (200–700 MPa) of silicon, indicating the cratering is caused by both these forces. The round device topographies are found to be less sensitive to cratering because of the lower stresses as verified by both experiments and simulations. Reinforcing the Al metal with a 1350-Å barrier metal layer improved the cratering performance because of reduction in compressive forces. However, further increasing the barrier metal thickness to 2000 Å did not improve the cratering performance due to the shearing stress caused cratering effects. Additionally, the change in stoichiometry of the BPSG layer caused cratering cannot be ruled out. The cratering rate on dimple topography had a direct correlation to the residual Al thickness and FAB size. With optimized bond parameter settings, the cratering rate can be significantly reduced from 100 k to 1 k ppm levels when the resulting residual Al thickness was greater than 0.65 μm.

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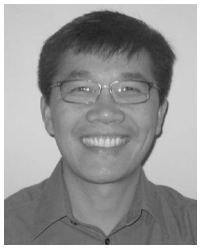

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Lu-Chang Qin, photograph and biography not available at the time of publication.