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Novel Si–Ge–C superlattices and their applications

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ABSTRACT

This paper presents Si–Ge–C superlattices (SLs) strained to Si that have direct band-gaps across a wide range of energies in the Infra-Red, dipole matrix elements larger than 1E−3, and oscillator strengths larger than 1E−1. Due to their constituents, these SLs will be able to be monolithically integrated with CMOS, thereby enabling efficient light emission and light absorption devices such as Light Emitting Diodes (LEDs), LASERs, and Photo-Diodes, in close proximity to CMOS devices. Key applications include Silicon Photonics, Multispectral CMOS Image Sensors, and Wide Spectrum PhotoVoltaic Cells, among others.

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1. Introduction

The development of efficient optical devices with Si-based technologies, suitable for monolithic integration with CMOS has been a goal for several decades. In order to achieve efficient light absorption and emission, it is necessary to have a direct band-gap and sufficiently large oscillator strengths. This is a general statement, regardless of the wavelength. For photonic circuitry and optical communications it is very desirable to have band-gap energies around 0.8 eV ($\lambda = 1.55$ μm) and smaller. For image sensing the entire Infra-Red (IR) range, from Short-Wavelength Infra-Red (SWIR), to Mid-Wavelength Infra-Red (MWIR) to Long-Wavelength Infra-Red (LWIR), is of high interest since different types of information can be extracted from the different wavelength ranges. With Multi-Junction PhotoVoltaic cells it is also very useful to be able to absorb photons in those IR regions, which are outside the range absorbed by Si and Ge, and which also enable to capture the "night glow" thereby generating electrical power during the night.

With CMOS technology approaching mesoscopic dimensions for the critical regions of MOSFETs [1], intra-chip and inter-chip optical interconnects have become key enablers to maintain the desirable trends captured by Moore's Law, and which were observable until recent CMOS generations. It is also important to note that the application of photonics for this purpose has requirements that differ considerably from those for conventional fiber optics communications [2].

Another major barrier to the desirable trends captured by Moore's Law, is the problem of power dissipation, which has led to the growing interest in Tunnel-MOSFETs, which offer a solution to this problem [3]. While the type of band offsets needed for Tunnel-NMOS can be obtained with SiGe random alloys strained to Si, the same is not true for the band offsets needed for Tunnel-PMOS. Also, it has been pointed out [4] that a key problem of Si and SiGe-based Tunnel-MOSFETs is the limited ON-state current due to the inefficiency of band-to-band tunneling processes inherent to indirect band-gap materials in which the top of the valence band (VB) and the bottom of the conduction band (CB) occur at different points of *k*-space.

Consequently, there are multiple important applications that can significantly benefit from monolithically integrated active regions with direct band-gaps and useful oscillator strengths. All this has led to the pursuit of several different approaches to achieving efficient light emission from Si-based devices, including: $(Si)_m$–$(Ge)_n$ SLs; defect engineering of states in the gap of Si; Er-doping of Si and/or SiO_2, epitaxial $FeSi_2$; tensile strained Ge; and GeSn alloys grown on Ge layers (often relaxed buffer layers grown on Si); and the integration of III/V materials with silicon.

Each of these approaches has different advantages and disadvantages, but most of them require the active regions to be epitaxially grown on buffer layers on Si substrates. In order to achieve lower defectivity levels, which are still typically larger than 1E6/cm^2, the buffer layers are usually more than 1 μm thick, which presents a major challenge for planarization, since for monolithic integration with contemporary, high-yielding, CMOS processes, the height of the MOSFETs is typically less than 200 nm.

Therefore it is very desirable to have alternative ways of achieving direct band-gaps having large oscillator strengths with materials and devices that can be pseudomorphically grown directly on a silicon active region, which is the case with the Si–Ge–C superlattices (SLs) described in the next sections.

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2. Background

2.1. Previous work on Si-based superlattices

Theoretical modeling of the $(Si)_m$–$(Ge)_n$ SLs [5], where "m" and "n" are, respectively, the number of atomic planes for Si and Ge, established that for SL crystals grown along the <100> direction, a direct band-gap could be obtained through zone folding of the $2\Delta_{\perp}$-valleys perpendicular to the substrate surface plane (i.e., parallel to the SL axis), if these were lowered (in energy) with respect to the in-plane 4Δ// -valleys, as shown in Fig. 1. For SLs made using only Si and Ge, this configuration could not be achieved with films grown pseudomorphically on Si, but could be achieved by placing Si layers under tensile strain [6], i.e., performing the epitaxial growth of the SL on a $Si_{1-x}Ge_x$ relaxed buffer, which would have the added benefit of allowing at least partial strain compensation. The already mentioned high defectivity of SiGe buffer layers was the likely reason for the previous absence of good $(Si)_m$–$(Ge)_n$ photo-diodes, LEDs, or LASERs, using this approach. However, recently Ge-based layers/devices, tensile strained to relaxed Ge buffer layers, have demonstrated lasing action [7].

Nonetheless, theoretical work on this type of SL continues, and SL compositions arrived at with genetic algorithms indicate that oscillator strengths larger than 1E−2 are possible [8].

The previous work on $(Si)_m$–$(Ge)_n$ SLs was performed almost exclusively on SLs grown on crystalline (100) surfaces. However, the CB of Si and CB of Ge have energy minima, respectively, along the X-direction and the L-directions of the Brillouin Zone (BZ). Different surface orientations lead to different alignments between the direction of strain and the directions of symmetry in the BZ. Consequently, the SL-constituent materials and the SLs can have very different band structures depending on the surface orientation on which the pseudomorphic growth takes place. The possibility of having silicon wafers with multiple sets of active areas, each with different crystalline orientation [9,10], enables the utilization of surface orientation as a tool for band structure engineering. However, there is much less experience in the epitaxial pseudomorphic growth of heterostructures on (110) or (111) surfaces than on (100) surfaces, which could delay the availability of high-quality SL layers on these surfaces.

2.2. Si–Ge–C superlattices

The splitting in the CB of Si can also be produced through the incorporation of carbon into the Si layers [11], i.e., with $Si_{1-y}C_y$ films strained to Si, as shown in Fig. 2.

Therefore, by taking $(Si)_m$–$(Ge)_n$ SLs and replacing the pure Si layers with $(Si_{1-y}C_y)$ alloys, the theoretical condition required for SLs with direct band-gaps is achieved with films pseudomorphic

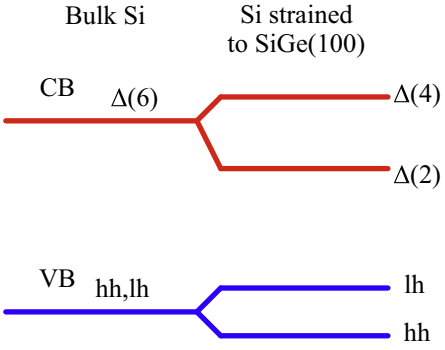

Fig. 1. Impact on the band edges of placing Si under tensile strain [see Ref. [6]].

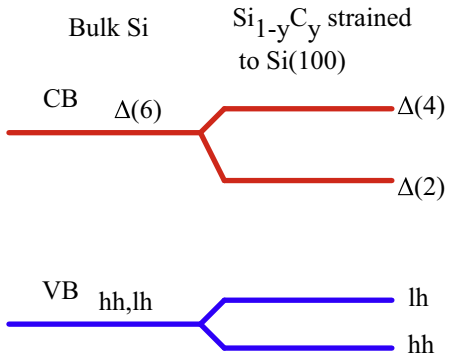

Fig. 2. Impact on the band edges from inserting C into the Si lattice ($Si_{1-y}C_y$ alloys) Ref. [11].

to the Si lattice constant. SLs strained to Si, of the form $(Si_{1-y}C_y)_m$–$(Ge)_n$, shown in Fig. 3, or $(Si_{1-y}C_y)_m$–$(Si_{1-x}Ge_x)_n$, can be grown directly on the surface of a CMOS active area, with the possibility of partial strain compensation depending on the combination of the amount of C and SL periodicity.

A schematic band diagram of a $(Si_{1-y}C_y)_m$–$(Ge)_n$, with 7% substitutional carbon in shown in Fig. 4, in which "m" and "n" are the number of atomic planes for the $Si_{1-y}C_y$ alloy and Ge, respectively, and the band offsets are obtained by the empirical expressions [11]:

$$\Delta E_g = -y \cdot ((6.5 \pm 0.3)\ \text{eV}),$$
$$\Delta E_C(\Delta 2) = -y \cdot E(4.6\ \text{eV}),$$
$$\Delta E_V(\text{lh}) = -y \cdot (1.9\ \text{eV}).$$

Conventionally, epitaxial $Si_{1-y}C_y$ layers are random alloys with fully substitutional carbon content up to only a few percent, which in the case of layers grown by CVD is approximately 3.2% or less [12]. However, it was demonstrated by MBE growth that Si_4C (20% C) *ordered alloys* can be pseudomorphic on Si [13,14]. Theoretical studies [15] have analyzed the precursor molecules for CVD growth, the corresponding crystal structures, and the band structures for Si_4C, as well as other ordered alloys with high C content. The band structures were not calculated for films strained to Si, but rather for "bulk" materials, relaxed to their natural lattice constants, which would require substrates with suitable lattice constants, a problem without an obvious solution.

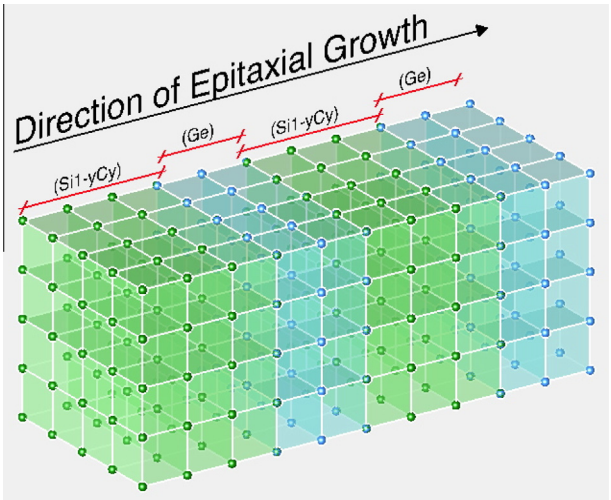

Fig. 3. Schematic of $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs.

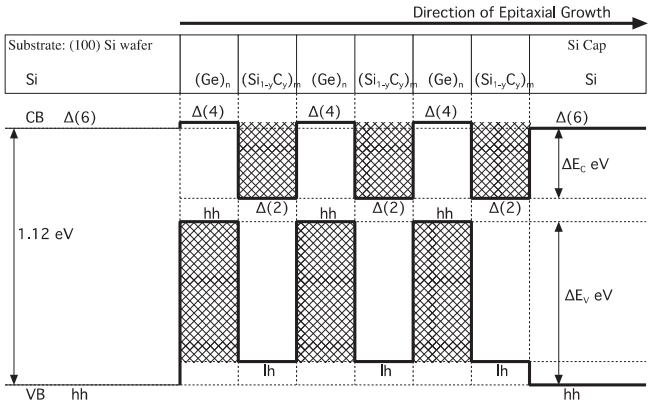

Fig. 4. Schematic band diagram of a $(Si_{1-y}C_y)_m$–$(Ge)_n$ SL strained to Si (100), for approximately y(substitutional) = 7%.

The lattice mismatch, relative to Si, of Si_4C is −8.1%, [15] while for Ge, it is +4.2%. These values make it impossible to grow thick pseudomorphic layers of Si_4C, but it is feasible to grow the few atomic planes necessary to construct short period SLs strained to Si. In addition, these ordered alloys have a larger critical thickness, at least 7 to 8 monolayers [13], than what one could expect from the lattice constant derived from Vegard's law [16].

Naturally, Si can be inserted into $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs, resulting in $(Si_{1-y}C_y)_m$–$(Ge)_n$–$(Si)_p$ strained to Si, thereby having an additional degree of freedom in band-gap engineering. $(Si_{1-y}C_y)_m$–$(Si)_n$ SLs strained to Si are also possible, but have lower critical thickness in view of the lack of strain compensation provided by Ge. This article reports only on band structures of $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs.

2.3. Ab-initio simulations of SL components

The band structures of the SLs were obtained with first-principles density-functional theory codes using plane-wave basis sets [17], and the Tran-Blaha functional for exchange–correlation potential [18].

The supercells representing different SL periodicities have different symmetries for the BZ due to zone folding, thereby requiring a different k-path and making it difficult for direct comparisons between the band structures of the different SL periodicities. A solution to this problem is to have band structures "unfolded" [19] to the fcc symmetry, which was the solution used for all band structures presented in this article. Also, given that SLs strained to (100) and (111) surfaces were studied, the k-path includes the 3 "X" directions (Δ-valleys) and the 4 "L" directions (Λ-valleys) of the BZ.

The credibility of the ab initio simulation results for the $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs is established by the results for the components of the SL, namely, Ge, Si, and $Si_{1-y}C_y$ alloys. Details about the ab initio simulation codes [20] and comprehensive band structure studies of Ge, Si, and $Si_{1-y}C_y$ alloys, strained to multiple surface orientations, along with respective band offsets relative to the substrates used, will be reported elsewhere [21]. The simulation code produces band-gap values for Si and Ge, at zero temperature, of 1.166 eV and 0.736 eV, as shown in Fig. 5 and Fig. 6, respectively, while the experimental values are 1.17 eV and 0.74 eV [22], respectively.

The band structures for Ge strained to Si (100) and Si (111) are shown in Fig. 7 and Fig. 8. It is interesting to note that Fig. 7 shows the CB minimum at the in-plane 4Δ-valleys, while Fig. 8 shows a near degeneracy of the 6Δ-valleys and 6L-points, with the

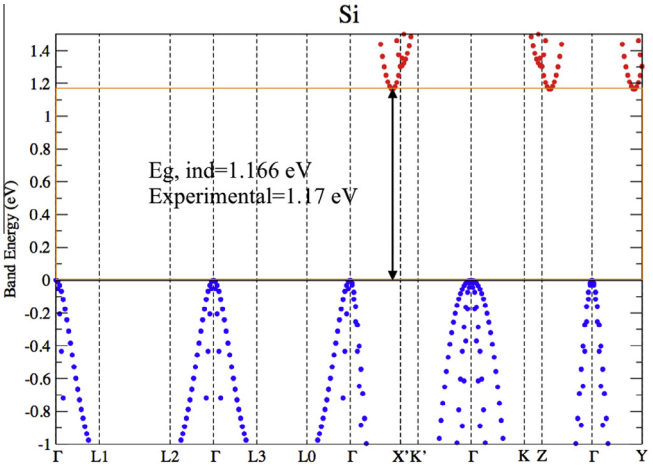

Fig. 5. Band structure of unstrained Si.

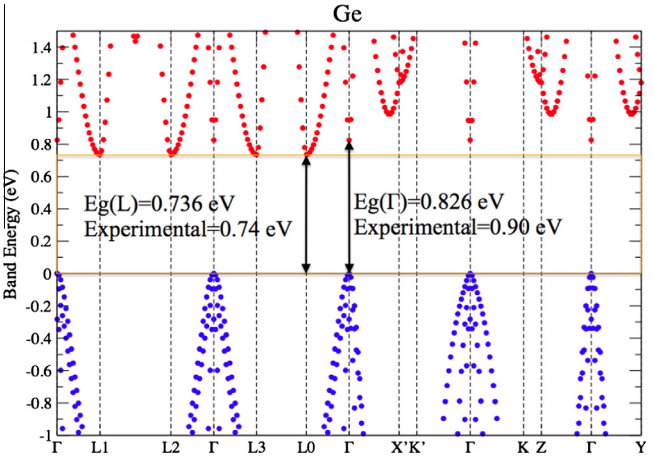

Fig. 6. Band structure of unstrained Ge.

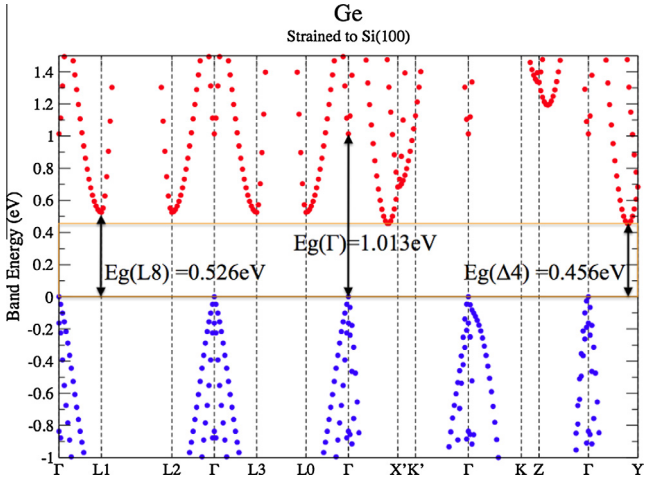

Fig. 7. Unfolded band structure of Ge strained to Si (100).

2Λ-valleys in the direction −L0 to +L0, corresponding to the direction of epitaxial growth, raised in energy.

Regarding $Si_{1-y}C_y$ alloys, pseudomorphic growth and characterization of such films strained to Si (111) has never been reported. Experimental data exists only for low carbon concentrations

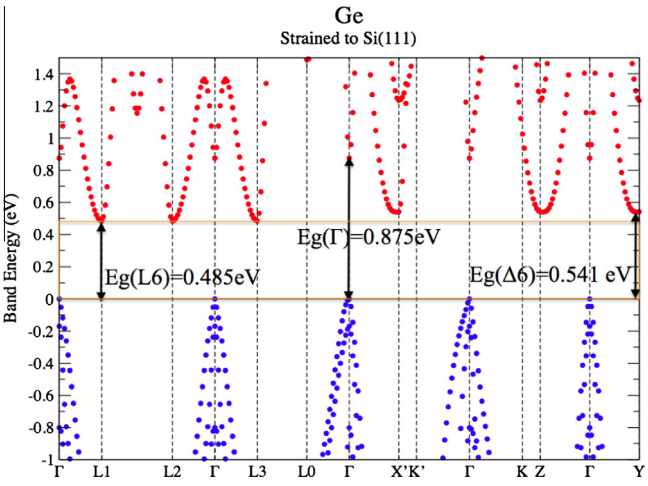

Fig. 8. Unfolded band structure of Ge strained to Si (111).

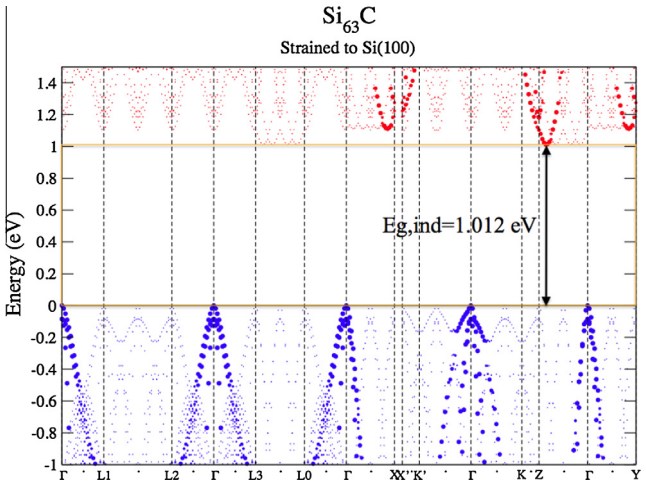

Fig. 9a. Unfolded band structure of $Si_{63}C$ strained to Si (100).

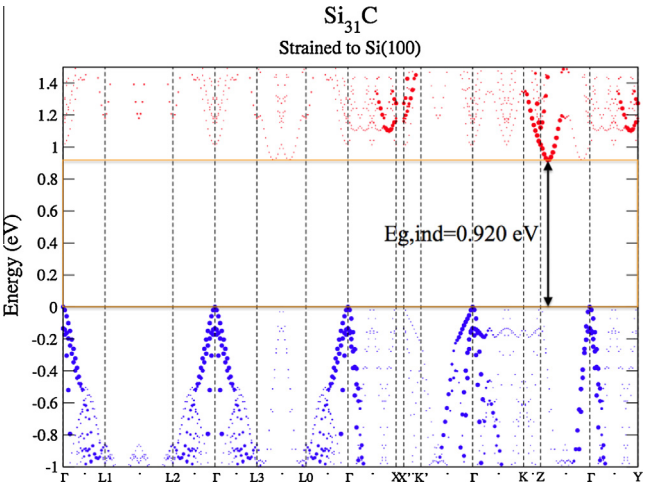

Fig. 9b. Unfolded band structure of $Si_{31}C$ strained to Si (100).

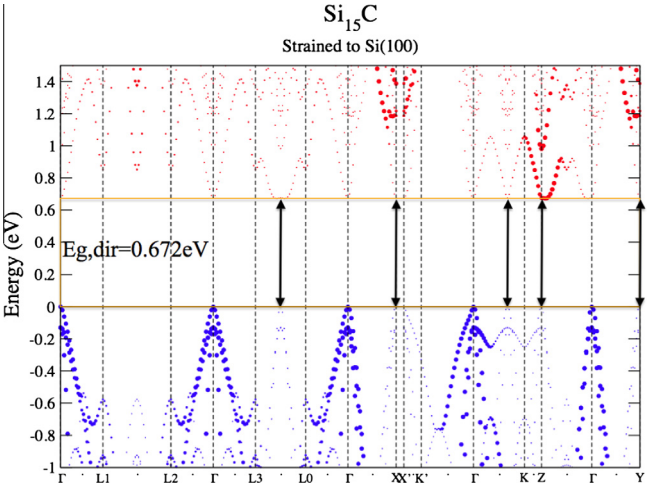

Fig. 9c. Unfolded band structure of $Si_{15}C$ strained to Si (100).

strained to Si (100), and the band-gap values produced by the ab initio simulations seem in reasonable agreement with the experimental data. The band-gap values derived from experimental data are calculated according to the formula $\Delta E_g = -y$ (6.5 ± 0.3) eV, which has only been verified for low carbon concentrations (<7%) [11].

The simulated and experimental results are summarized in Table 1. It should be kept in mind that the simulated results are for *ordered alloys* and the experimental data is from *random alloys*. The corresponding band structures are shown in Figs. 9A - 9C

It is interesting to note that the true ab initio results reported in this paper show Si_4C (y = 20%) as being a semiconductor with a gap of 0.512 eV when strained to Si (111), shown in Fig. 10A, and a semimetal with a negative band-gap of −0.256 eV when strained to Si (100), shown in Fig. 10B.

Previous studies [23] of $Si_{1-y}C_y$ alloys strained to Si (100) indicated that increasing the carbon concentration up to 12.5% would reduce the band-gap, which at 12.5% was negative (metallic), but at higher concentrations was found to increase again. The ab initio results reported in this paper show that the gap shrinks with increasing carbon content, at least up to 20% C.

Another interesting result, shown in Fig. 9C, is that for certain carbon concentrations, ordered alloys have direct band-gaps with meaningful oscillator strengths, as had been predicted [24].

Although the critical thickness of pure Ge and $Si_{1-y}C_y$ alloys (with high C%) strained to Si is just a few atomic planes, it is sufficient for short-period SLs.

2.4. Ab-initio simulations of $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs

Due to the computational burden of pseudopotential plane wave simulations, in which the computational time increases with N^3 and memory requirements increase with N^2, where N is the total number of atoms in the supercell, it is extremely important to minimize the number of atoms in the supercells to be simulated.

Table 1
Simulated and experimental data for the band-gap reduction in $Si_{1-y}C_y$ alloys.

E_g	Ab-initio (eV)	Exp. (eV)
y = 0 (pure Si)	1.166	1.17
y = 1.5625%	1.012	[1.064–1.073]
y = 3.125%	0.920	[0.957–0.976]
y = 6.25%	0.672	[0.745–0.783]

For this reason, the chosen $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs for ab initio simulations are the ones with the smallest number of atoms per atomic plane. All atomic planes must have the same number of

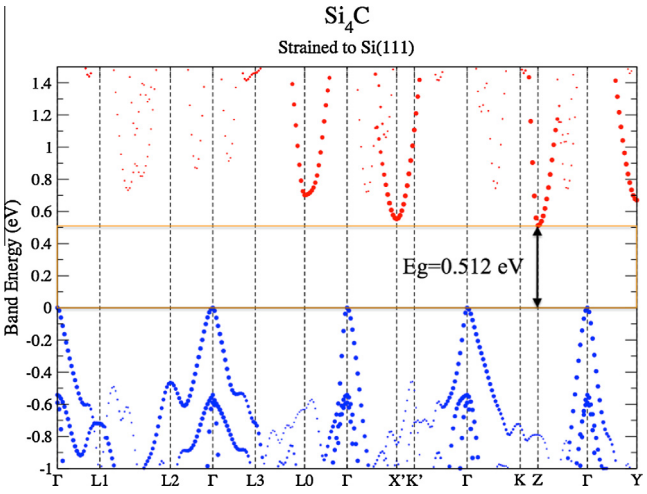

Fig. 10a. Unfolded band structure of Si_4C strained to Si (111).

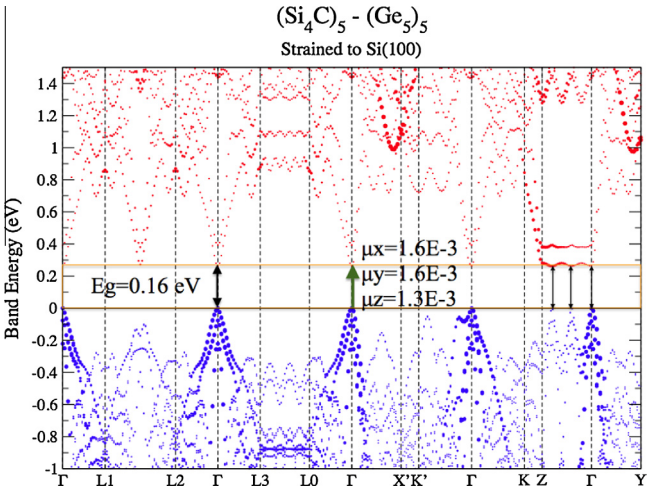

Fig. 11. Unfolded band structure of $(Si_4C)_5$–$(Ge_5)_5$ strained to Si (100).

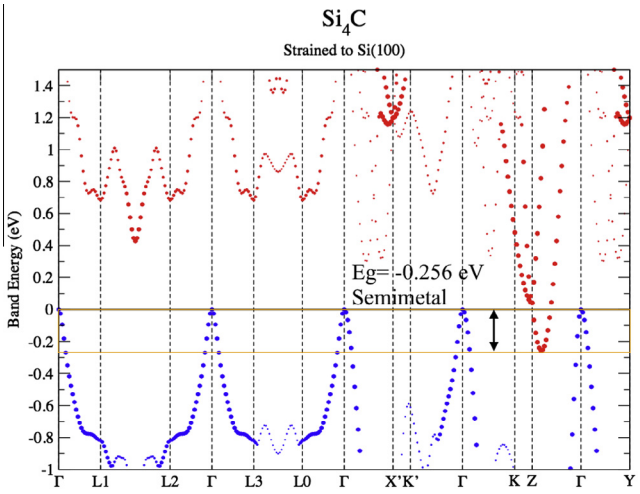

Fig. 10b. Unfolded band structure of Si_4C strained to Si (100).

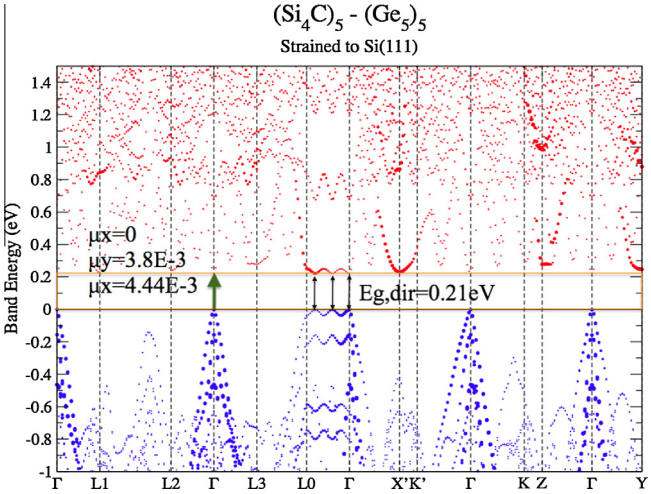

Fig. 12. Unfolded band structure of $(Si_4C)_5$–$(Ge_5)_5$ strained to Si (111).

atoms, which corresponds to the minimum number of atoms necessary to describe the most dilute stoichiometry in the entire stack of atomic planes. For the type of SL studied here, this means that the minimum number of atoms for the atomic planes is determined by the carbon content of the $Si_{1-y}C_y$ alloys. The compositions that require fewer number of atoms are the ones with the highest carbon content, i.e., Si_4C, which requires 5 atoms per atomic plane. In this case, the supercell describing this configuration must also have 5 Ge atoms per atomic plane, and in the descriptive nomenclature used here, this will be denominated as $(Si_4C)_m$–$(Ge_5)_n$, with the total number of atoms in the SL as $N = 5(m + n)$.

The SL axis is formed along the z-direction (of epitaxial growth) and the dipole matrix element $\mu = |\langle v|dH/dk|c\rangle|^2$, calculated for the z-direction (μz) refers to light propagating parallel to the substrate surface. Dipole matrix elements calculated for the x- and y-directions (μx and μy) refer to light propagating parallel to the SL axis. The combinations of different "m" and "n" and the surface orientations, result in a fairly large number of SL compositions. The following are a few examples of SLs with direct band-gaps and non-zero oscillator strengths, for at least one direction of polarization.

The same SL composition, $(Si_4C)_5$–$(Ge_5)_5$, but strained to Si (100) and Si (111), Fig. 11 and Fig. 12 respectively, has slightly

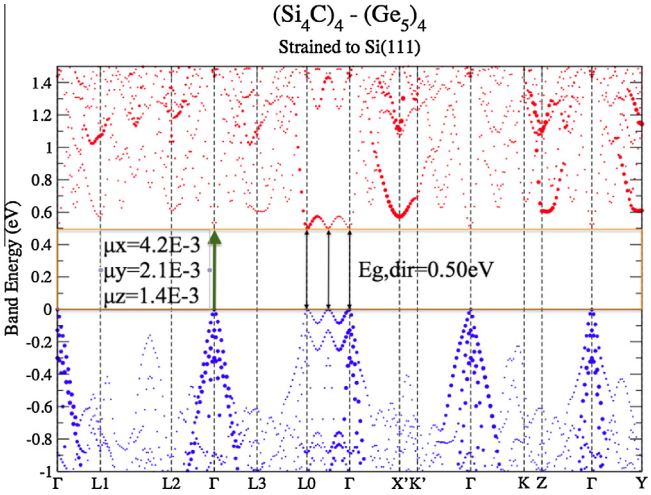

Fig. 13. Unfolded band structure of $(Si_4C)_4$–$(Ge_5)_4$ strained to Si (111).

different band-gap values, 0.156 eV for the former and 0.207 eV for the latter, and also slightly different dipole matrix elements. As expected, shorter period SLs have larger band-gaps, 0.5 eV for

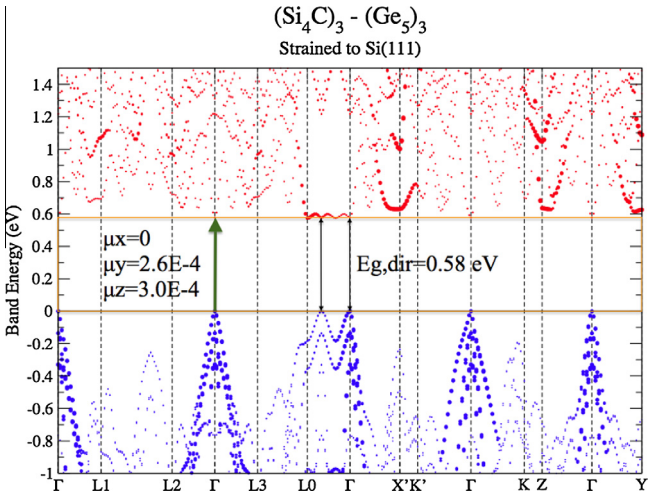

Fig. 14. Unfolded band structure of $(Si_4C)_3$–$(Ge_5)_3$ strained to Si (1 1 1).

$(Si_4C)_4$–$(Ge_5)_4$, shown in Fig. 13 and 0.578 eV for $(Si_4C)_3$–$(Ge_5)_3$, shown in Fig. 14.

Table 2 shows the dipole matrix elements and oscillator strengths (f), with $f = (2/3) * (1/Eg) * \mu$, which are in general significantly different for the each direction of polarization. For all SLs, the axis of the SL is along the z direction.

Several of these examples have oscillator strengths lager than 1E−1, which are similar to those obtainable with $(Si)_m$–$(Ge)_n$ SLs strained to SiGe buffers layers [8], and deemed sufficiently large for efficient optical devices such as LEDs and LASERs, in addition to photo-diodes with much higher quantum efficiencies than those obtainable with SiGe alloys strained to Si.

2.5. Fabrication

As the simulations show, the band structure of the SLs is sensitive to the exact composition and therefore the fabrication of SLs with reproducible properties requires reliable control of the composition of the atomic planes in the SLs. Therefore it is important to address the two most obvious sources of concern regarding the fabrication of Si–Ge–C SLs.

The ideal fabrication method of these SLs utilizes self-limiting epitaxial growth, in which the composition of the SL layers can be controlled on an atomic-plane by atomic-plane fashion. This capability has been demonstrated for group-IV materials utilizing semiconductor production equipment [25,26]. However, it is recognized that self-limiting growth may present a significant challenge regarding the deposition time for total thickness of a SL, compared to the deposition time for conventional SiGeC random alloys. Therefore it is likely that the CVD reactor hardware will need to be optimized in order to produce suitable growth rates, while using the precursors that can deliver the desired SL compositions.

As it is typical in the ab initio simulations of this type of structures, the structural cells are idealized models of the materials, and did not take into account defects, vacancies, interstitials, step edges, surface roughness, chemical intermixing at the interfaces, etc. Perhaps the most critical of these factors is surface roughness, which is known to disrupt layer compositions and potential profiles in the plane of the surface, and perpendicularly to the surface. In order to avoid these detrimental effects, the surface of the Si active area on which the epitaxial growth takes place should be a mono-terrace surface [27]. The processing needed to produce such a surface is fairly straightforward [28] and is compatible with conventional processing of CMOS [29] and CMOS Image Sensors [30], while also benefiting from a reduction in the lateral dimensions of the active area.

2.6. Applications

SLs with direct band-gaps may allow the monolithic integration with CMOS of LEDs, LASERs, and Photo-Diodes, thereby enabling Silicon Photonics without the hybrid integration of III/V LASERs. Direct band-gaps also enable very efficient multispectral image sensing and wide spectrum photovoltaic cells.

2.6.1. Complementary tunnel MOSFETs

Tunnel heterojunction MOSFETs promise ultra-low voltage operation [3], but suffer from low ON-state current due to the low efficiency of band-to-band tunneling in indirect band-gaps of source-to-channel heterojunctions [4]. Devices made on ultra-thin SOI substrates, have an ON-state current much closer to that of Thermionic-MOSFETs, although the physics behind this enhancement has not been discussed in detail [31]. The required band offsets for Tunnel-PMOS also do not exist for SiGeC alloys strained to Si. Si–Ge–C SLs with direct band-gaps can offer high ON-state current and, with a wide range of band offsets, may enable the realization of complementary tunnel devices with epitaxial layers pseudomorphic on Si surfaces.

The replacement of Thermionic-MOSFETs by Tunnel-MOSFETs operating at 0.2 V or lower, is likely to occur for the 10 nm or 7 nm ITRS nodes, and requires high quality source/channel heterojunctions for both the NMOS and PMOS devices. Fabricating such heterojunctions with channel lengths on the order of a few nanometers is extremely challenging for devices in which the critical dimensions, such as gate/channel length, are defined by lithography and etching, as in conventional horizontal devices and also FinFETs.

However, it is much more straightforward for vertical devices, in which the source, channel and drain regions are grown epitaxially. In vertical devices, the epitaxial process can be used to control the channel length through heterojunction and/or doping profiles, without diffusion, and therefore with atomic layer control of the critical dimensions, something that is impossible to achieve with lithography-based processes. In the past, it was argued that because the channel length is fixed by epitaxy for all devices, this was not acceptable to circuit designers. However, the major CMOS foundries introduced rigid layout rules for (conventional) 20 nm processes, in which the key dimensions of the MOSFETs cannot be changed by the circuit designers.

Therefore, vertical MOSFETs are the best candidates to achieve the ultimate MOSFET scaling, implementing tunnel injection from source to channel, and with atomic-layer control of the critical

Table 2
Dipole matrix elements for the different directions of polarization, between the conduction band minimum and the valence band maximum of the different superlattices.

SL	Substrate	Eg (eV)	$\mu(x)$	$\mu(y)$	$\mu(z)$	μ	f
$(Si_4C)_5$–$(Ge_5)_5$	Si (1 0 0)	0.156	2.52E−03	1.62E−03	1.3E−03	4.62E−03	5.16E−01
$(Si_4C)_5$–$(Ge_5)_5$	Si (1 1 1)	0.207	0	3.8E−03	4.44E−03	8.3E−03	7.07E−01
$(Si_4C)_4$–$(Ge_5)_4$	Si (1 1 1)	0.504	4.2E−03	2.1E−03	1.42E−03	7.7E−03	2.76E−01
$(Si_4C)_3$–$(Ge_5)_3$	Si (1 1 1)	0.58	0	2.6E−04	3.0E−04	5.4E−04	1.68E−02

dimensions of the device. Vertical MOSFETs are also the ideal architecture to implement Tunnel-CMOS in which the Si–Ge–C SLs strained to Si can be used in the source, and/or channel and/or drain regions, keeping in mind that the best band offsets for Tunnel-NMOS and for Tunnel-PMOS, might be obtainable for SLs grown pseudomorphically on different Si orientations, as shown in Fig. 15.

2.6.2. Light-sensing in CMOS image sensors

Another key application for Si–Ge–C SLs is light sensing with photo-diodes in which the absorption region comprises one or more SLs with direct band-gaps. The SLs described in this paper have a range of direct band-gaps that cover large portions of the IR spectrum well beyond what Ge and InGaAs can cover, as is the case with $(Si_4C)_5$–$(Ge_5)_5$ strained to Si (1 1 1), shown in Fig. 12, with a gap of 0.23 eV, corresponding to a wavelength cutoff of 5.63 μm, already in the Mid-IR range.

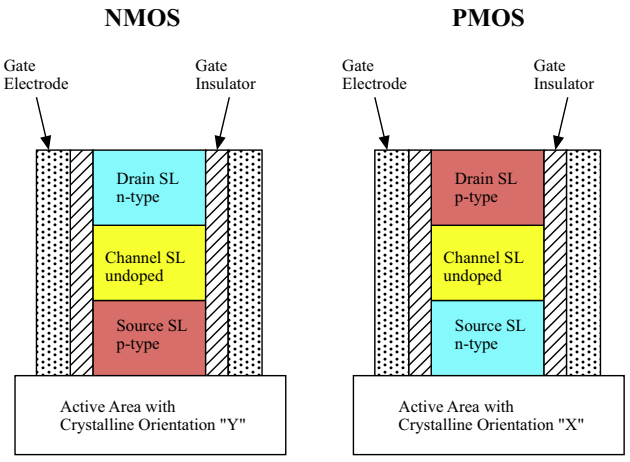

Fig. 15. Schematic of vertical tunnel-CMOS implemented with Si–Ge–C SLs for the source, channel and drain regions.

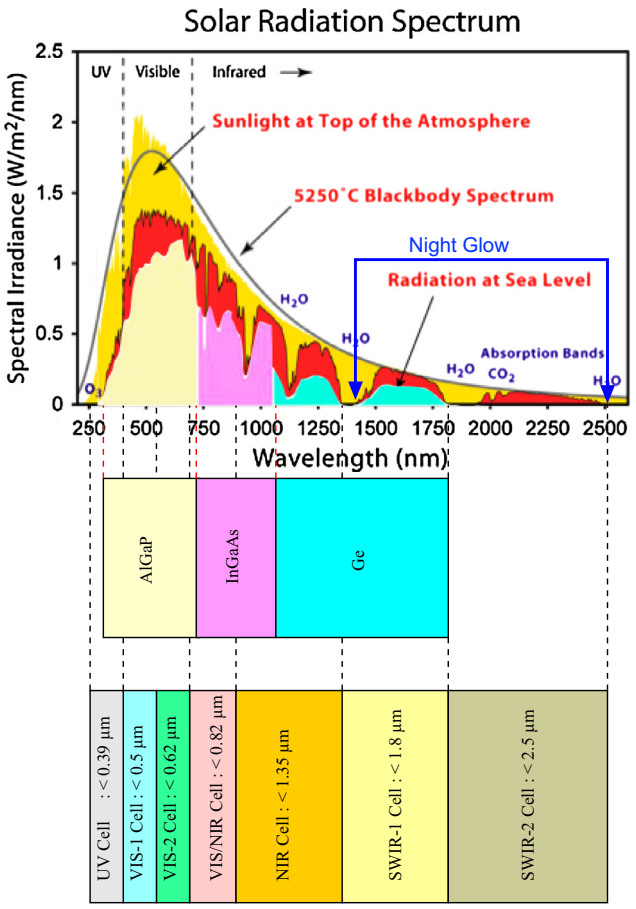

Fig. 18. Schematic of multi-junction cell incorporating Si–Ge–C SL layers.

Given that SLs are by their own construction anisotropic, and as can be verified by the oscillator strengths shown in Table 2, there can be orders of magnitude difference between different

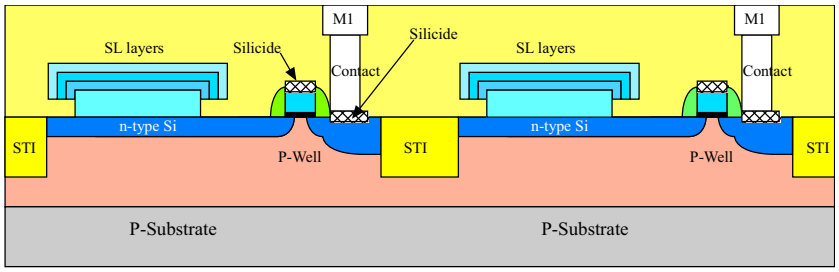

Fig. 16. Schematic of monolithic integration of Si–Ge–C SL layers with CMOS.

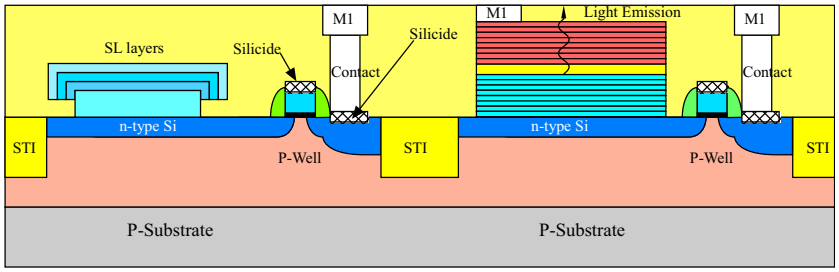

Fig. 17. Schematic of monolithic integration of Si–Ge–C SLs with CMOS for an optical transceiver.

polarizations. This anisotropy could be problematic for certain applications in which light should be absorbed in a photo-diode, regardless of polarization. This can be achieved with Selective Epitaxial Lateral Overgrowth, in which the epitaxial growth front progresses in 3D, thereby producing a material in which the SL-axis exists along the 3 main spatial directions. These Si–Ge–C SL layers can be monolithically integrated with CMOS in a very straightforward manner [32], as schematically shown in Fig. 16. Since all regions of the photo-diode can be grown epitaxially, it can be made independent of the substrate used to fabricate the CMOS devices, and is thus compatible with Silicon-on-Insulator (SOI) substrates, including Ultra-Thin Film (Fully Depleted) SOI [33].

2.6.3. Optoelectronic transceivers

It is anticipated that the biggest impact of Si–Ge–C SLs with direct band-gaps and large oscillator strengths may be for silicon-based LEDs and LASERs, monolithically integrated with CMOS, for silicon photonics. Monolithic integration is anticipated to enable a big leap forward in performance and power consumption [34].

An exemplary schematic cross section of CMOS devices monolithically integrated with a VCSEL with a Si–Ge–C SL active region, and a Si–Ge–C photo-diode, the key devices to build complete CMOS-based transceivers for optical communications (the different device layers are not to scale), is shown in Fig. 17. The SL layers of the photo-diode and for the LASER can be grown in separate epitaxial runs.

2.6.4. Multi-junction photovoltaic cells

Another application with a potential high impact is Multi-Junction PhotoVoltaic (PV) Cells, as schematically shown in Fig. 18.

Since Si–Ge–C SLs offer the ability to cover a much wider range of the solar spectrum than Si and Ge, the overall efficiency of silicon-based PV cells is increased. In essence Si–Ge–C SLs can cover the regions of the solar spectrum for which InGaAs and Ge are currently used, with the advantage of being epitaxially grown directly on silicon substrates, with consequent benefits in terms of manufacturing infrastructure and cost for the PV cells.

3. Conclusions

With the Si–Ge–C superlattices grown pseudomorphically on Si substrates as described in this paper, the nature of the band-gap, whether direct or indirect, as well as it is magnitude and band offsets relative to Si, can vary significantly across the entire infra-red spectrum depending on the SL composition, periodicity, and surface orientation. Devices that until now have required compound semiconductors may now be possible to implement with Si–Ge–C SLs, which are compatible with standard CMOS processing. A few applications, such as Tunnel-CMOS, Photo-diodes & LASERs for optical transceivers, and wide spectrum PhotoVoltaic Cells, have the potential for high impact in the near future. For each of these types of applications, the benefits are multiple and include the enablement of higher performance, higher efficiency, and increased functionality.

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